Abstract

An apparatus, for use in a semiconductor device, for providing a domain crossing operation. The apparatus includes a domain crossing sensing block, in response to an operation mode signal, first and second delay locked loop (DLL) clock signals and a CAS latency, generates a plurality of selection signals. An output enable signal generator, in response to the plurality of selection signals, generates a plurality of output enable signals. A data control block, in response to the output enable signals and the CAS latency, controls a data output operation in the semiconductor device. Each of a plurality of data align block, in response to the selection signals, the first and second DLL clock signals and an address signal, aligns data corresponding to the address signal in the data output operation.